AMENDMENTS TO THE CLAIMS

The following Listing of Claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A process for manufacturing a silicon-on-insulator wafer comprising the steps of:

~~(a)~~ providing a silicon substrate;

~~(b)~~ forming an oxide insulator layer across the wafer by oxygen implantation, the insulator layer being buried within the silicon substrate, dividing the silicon substrate from a top silicon layer, and having a top surface and a bottom surface;

~~(c)~~ thickening the insulator layer by reducing one or more of the implantation dose, energy, and temperature;

~~(d)~~ creating at least one of a contoured top surface and a contoured bottom surface of the insulator layer by adjusting one or more of the implantation dose, energy, and temperature; and

~~(e)~~ annealing to further thicken and contour the insulator layer.

2. (Currently amended) The process of claim 1 wherein the step ~~(b)~~ of forming an oxide insulator layer across the wafer by oxygen implantation is accomplished using a qualified oxygen implanter.

3. (Canceled)

4. (Currently amended) The process of claim 1 wherein the step ~~(e)~~ of annealing is an oxygen anneal.

5. (Original) The process of claim 1 wherein the at least one contoured surface is uniformly convex.

6. (Currently amended) The process of claim 5 wherein the step ~~(b)~~ of forming an oxide insulator layer across the wafer by oxygen implantation is accomplished using a qualified oxygen implanter and the step ~~(d)~~ of creating the at least one uniformly convex surface includes reducing one or more of the implant dose, energy, and temperature to thicken the insulator layer across a preset diameter that is less than the diameter of the wafer.

7. (Original) The process of claim 1 wherein the at least one contoured surface has alternating convex and substantially flat regions.

8. (Original) The process of claim 1 wherein the at least one contoured surface is uniformly concave.

9. (Currently amended) The process of claim 8 wherein the step ~~(b)~~ of forming an oxide insulator layer across the wafer by oxygen implantation is accomplished using a qualified oxygen implanter and the step ~~(d)~~ of creating the at least one uniformly concave surface includes reducing one or more of the implant dose, energy, and temperature to thicken the

insulator layer around the wafer in a donut area having an outer diameter not exceeding the diameter of the wafer an interior diameter greater than zero.

10. (Original) The process of claim 9 further comprising adjusting the implanter to scan only the donut region around the wafer within preset diameters.

11. (Original) The process of claim 1 wherein the at least one contoured surface has alternating concave and substantially flat regions.

12. (Original) The process of claim 1 wherein the at least one contoured surface includes a combination of convex, concave, and substantially flat portions.

13. (Currently amended) The process of claim 12 wherein the step ~~(b)~~ of forming an oxide insulator layer across the wafer by oxygen implantation is accomplished using a qualified oxygen implanter and the step ~~(d)~~ of creating the at least one contoured surface includes reducing one or more of the implant dose, energy, and temperature to selectively pattern the buried insulator layer with topography at predetermined coordinates.

14. (Currently amended) A process for manufacturing a silicon-on-insulator wafer comprising the steps of:

~~(a)~~ providing a silicon substrate;

~~(b)~~ forming an oxide insulator layer across the wafer by oxygen implantation, the insulator layer being buried within the silicon substrate, dividing the silicon substrate from a top silicon layer, and having a top surface and a bottom surface;

~~(c)~~ thickening the insulator layer by reducing one or more of the implantation dose, energy, and temperature;

~~(d)~~ generating the chip periodicity for the wafer and setting the coordinates where a predetermined topography of the buried oxide insulator layer is desired;

~~(e)~~ transferring the coordinates to an oxygen implanter for implementation;

~~(f)~~ adjusting the energy, dose, or temperature of the oxygen implant with the implanter scanning and the wafer tilting or rotating according to preset coordinates from the chip periodicity map at the predetermined thicknesses and contours required, thereby creating at least one of a contoured top surface and a contoured bottom surface of the insulator layer; and

~~(g)~~ annealing to further thicken and contour the insulator layer.

15-20 (Canceled)